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10/824,504	04/15/2004	Yuichiro Morita	500.40687CX1	6566

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EXAMINER	
SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,504	MORITA ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/ are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed November 30, 2007 in response to the Office action dated May 31, 2007. Claims 1-5 have been amended. New claims 6-10 have been added. Claims 1-10 are pending in this application.

OBJECTIONS

1. **Claim 3** is objected to because there should be no space between the last word and the period on the last line of the claim.

2. **Claim 5** is objected to because on line 8 of the claim the limitation "said page" should instead read "said second page."

3. **Claim 8** is objected to because the claim should depend on claim 3, not claim 6.

4. **Claim 10** is objected to because the claim recites the limitation "said memory control means includes means for executing" on lines 1-2, however, there is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending the claim to instead read "said memory control unit is further adapted to execute."

Appropriate correction is required.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Jones et al. (U.S. Patent 6,233,661) (hereinafter "Jones").

7. **As per claim 1**, Jones discloses a memory controller comprising:

means for receiving, from a processor, a request for access to a single dynamic random access memory (col. 9, lines 56-60; Fig. 4A, element 304) having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 5, lines 53-61; col. 12, lines 35-38; Fig. 4B, element 106); *It should be noted that pg. 15, lines 3-5 of Applicant's specification appear to define this means as an "access arbiter." Jones' "MEMARB" is equivalent to Applicant's "access arbiter." It should also be noted that Jones' "CPU" is equivalent to Applicant's "processor."*

and memory control means for activating a first page to be accessed, based on said access request from said processor, and executing, before a next request for access to a second page to be accessed subsequently by said processor, precharge of said second page to be accessed subsequently (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 4A, element 308; Figs. 7 and 8). *It should be noted that pg. 30, line 17 – pg. 31,*

line 5 appear to define this control means a "memory control unit." Jones' "SDRAMSM" is equivalent to Applicant's "memory control unit." Also, please see the italicized citation notes for the limitation above regarding Jones' CPU.

wherein said plurality of banks are formed on a single chip (col. 5, lines 53-54; Fig. 4B, element 106), and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks (Fig. 4B, element 106 and control lines "RAS", "OUTPUT ENABLE", and "CKE"). *It should be noted that "**a** memory device" discloses that Jones' memory 106 is on a single chip, as opposed to "**an array** of memory devices."*

8. **As per claim 2**, Jones discloses a memory controller comprising:

means for receiving, from a processor, a request for access to a single dynamic random access memory (col. 9, lines 56-60; Fig. 4A, element 304) having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 5, lines 53-61; col. 12, lines 35-38; Fig. 4B, element 106); *Please see the italicized citation notes for the first limitation of claim 1 above.*

and memory control means for activating a first page to be accessed, based on said access request from said processor, and executing, before a next request for access to a second page to be accessed subsequently by said processor, precharge of a bank corresponding to said second page to be accessed subsequently (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 4A, element 308; Figs. 7 and 8). *Please see the italicized citation notes for the second limitation of claim 1 above.*

wherein said plurality of banks are formed on a single chip (col. 5, lines 53-54; Fig. 4B, element 106), and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks (Fig. 4B, element 106 and control lines "RAS", "OUTPUT ENABLE", and "CKE"). *Please see the italicized citation notes for the third limitation of claim 1 above.*

9. **As per claim 3**, Jones discloses a memory controller for use with a processor and a dynamic access memory, comprising:

a terminal adapted to receive a request for access from said processor to a single dynamic random access memory (col. 9, lines 56-60; Fig. 4A, element 304) having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 5, lines 53-61; col. 12, lines 35-38; Fig. 4B, element 106); *It should be noted that Jones' "MEMARB" is equivalent to Applicant's "terminal." Also, please see the italicized citation notes for the first limitation of claim 1 above.*

and memory control means for issuing an active command for activating a first page to be accessed, based on said access request from said processor, and issuing a precharge command for executing, before a next request for access to a second page to be accessed subsequently by said processor, precharge of said second page to be accessed subsequently (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 4A, element 308; Figs. 7 and 8). *It should be noted that Jones' "Activate command A" is equivalent to Applicant's "active command." Also, please see the italicized citation notes for the second limitation of claim 1 above.*

wherein said plurality of banks are formed on a single chip (col. 5, lines 53-54; Fig. 4B, element 106), and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks (Fig. 4B, element 106 and control lines "RAS", "OUTPUT ENABLE", and "CKE"). *Please see the italicized citation notes for the third limitation of claim 1 above.*

10. **As per claim 4**, Jones discloses a memory controller for use with a processor and a dynamic access memory, comprising:

a terminal adapted to receive a request for access from said processor to a single dynamic random access memory (col. 9, lines 56-60; Fig. 4A, element 304) having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 5, lines 53-61; col. 12, lines 35-38; Fig. 4B, element 106); *Please see the italicized citation notes for the first limitations of claims 1 and 3 above.*

and memory control means for issuing an active command for activating a first page to be accessed, based on said access request from said processor, and issuing a precharge command for executing, before a next request for access to a second page to be accessed subsequently by said processor, precharge of a bank corresponding to said second page to be accessed subsequently (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 4A, element 308; Figs. 7 and 8). *Please see the italicized citation notes for the second limitations of both claim 1 and claim 3 above.*

wherein said plurality of banks are formed on a single chip (col. 5, lines 53-54; Fig. 4B, element 106), and wherein said random access memory is adapted to share

control signals received by said random access memory, from said memory control means, among said plurality of banks (Fig. 4B, element 106 and control lines "RAS", "OUTPUT ENABLE", and "CKE"). *Please see the italicized citation notes for the third limitation of claim 1 above.*

11. **As per claim 5**, Jones discloses a memory controller comprising:

a terminal adapted to receive a request for access from said processor to a single dynamic random access memory (col. 9, lines 56-60; Fig. 4A, element 304) having a data storage area divided into a plurality of banks each divided into a plurality of pages (col. 5, lines 53-61; col. 12, lines 35-38; Fig. 4B, element 106); *Please see the italicized citation notes for the first limitations of claims 1 and 3 above.*

and a memory control unit adapted to activate a first page to be accessed, based on said access request from said processor, and to execute, before a next request for access to a second page to be accessed subsequently by said processor, precharge of said second page to be accessed subsequently (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 4A, element 308; Figs. 7 and 8). *It should be noted that Jones' "SDRAMSM" is equivalent to Applicant's "memory control unit." Also, please see the italicized citation notes for the second limitation of claim 1 above.*

wherein said plurality of banks are formed on a single chip (col. 5, lines 53-54; Fig. 4B, element 106), and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks (Fig. 4B, element 106 and control lines "RAS",

"OUTPUT ENABLE", and "CKE"). *Please see the italicized citation notes for the third limitation of claim 1 above.*

12. **As per claims 6-10**, Jones discloses said memory control means includes means for executing a precharge of said second page during a time period between a read operation of said first page and the request for access to the second page (col. 16, lines 1-15; Figs. 7 and 8). *It should be noted that even though Figs. 7 and 8 are for a write operation of the first page, in Jones the same precharging method is used by the memory controller for both read cycles and write cycles (col. 3, lines 53-55).*

Response to Arguments

13. Applicant's arguments with respect to **claims 1-10** have been considered but are moot in view of the new ground of rejection above.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-10** have received a second action on the merits and are subject of a second action final.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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February 7, 2008

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